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A FAST TRANSIENT CAPACITOR-LESS LDO REGULATOR WITH ACTIVE FREQUENCY COMPENSATION

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ABSTRACT

This paper introduces a low dropout (LDO) regulator designed for system-on-chip applications, operating without an external output capacitor. The design uses a folded cascode amplifier and an active capacitor circuit with a fast comparator to detect the offset voltage at the output in order to increase DC gain. As a result, the LDO regulator can quickly charge and discharge, the load capacitor and improving transient response while maintaining circuit stability. Furthermore, a nested miller compensation mechanism is used to stabilize the internal feedback loop under changing load conditions. The proposed LDO regulator implemented using 180 nm CMOS technology and can drive a peak load current of 50 mA while maintaining a stable output voltage of 1.6 V from a power supply voltage of 1.8 V.

1. INTRODUCTION

Low dropout regulators are critical components in modern power management electronic systems (Day, 2016; Manikandan et al., 2021a), notably because of their ability to maintain a *stable* output voltage despite variations in input unregulated voltage and load currents. These devices are critically important in battery-operated devices and systems-on-chip (SoC) applications, where efficient energy use and space constraints are prioritized. Traditional LDOs rely on large output capacitors to enhance performance metrics such as stability (phase margin, gain margin) and transient response (settling time, response time, and output voltage spike). However, integrating these external capacitors can be counterproductive in SoC applications that demand miniaturization.

Recent advancements in LDO regulator design have centered on maintaining performance and stability without the use of external output capacitors. Innovative compensation techniques, such as active feed-forward compensators that employ Miller capacitance (MC) with NMOS pass transistors, have been explored to stabilize the feedback loop and enhance transient responses, effectively shifting significant LHP zeros to stabilize the feedback loop under various load conditions (Laker & Sansen, 1994). Additionally, the implementation of bootstrap flipped-voltage followers (FVF) has shown significant improvements in both stability and transient response, facilitating effective operation without external capacitive components (Rogers, 1999).

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Other studies have introduced fast local feedback loops combined with overshoot detection mechanisms, addressing the need for rapid dynamic adjustments typical in capacitor-less LDO regulator configurations (Tiikkainen & Rahkonen, 2014). The application of nested Miller compensation techniques has also been noted for extending the operable load range of LDOs by optimizing feedback networks to improve phase margin, gain margin and frequency response (Chong, 2014). Moreover, specific solutions for output voltage spike detection and correction have been developed to mitigate transient voltage spikes common in designs lacking output capacitors (Hanumolu, 2015).

Building upon these foundational strategies, this paper presents a detailed exploration of a three-stage LDO regulator architecture designed to operate without an external output capacitor while ensuring robust stability and fast transient response. The design begins with a P-MOS folded cascode amplifier, chosen for its high gain and high bandwidth, which enhances the performance of the error amplifier (EA). This is followed by a basic common-source amplifier, which boosts the DC gain and considerably improves overall system stability. The last step includes an active capacitor circuit with a quick comparator that senses the offset voltage at the output. As a result, the LDO regulator can swiftly charge and discharge the external load capacitor, improving transient response while preserving the stability of the LDO regulator circuit. Additionally, the Miller compensation method with a feed-forward capacitor is implemented to stabilize the internal feedback loop under varying load conditions. The developed LDO regulator is expected to overcome typical design challenges, offering a stable and efficient power supply solution suitable for advanced integrated circuits and SoC applications. This approach not only echoes the advancements discussed but also sets a new benchmark in the design and implementation of capacitor-less LDO regulators for modern power management electronic devices.

The suggested work is divided into seven sections. Section 1 provides an introduction, while Section 2 describes the traditional LDO regulator. The suggested LDO regulator is explained in Section 3. In Section 4, the stability of the suggested LDO regulator is examined. The LDO regulator's transient response is explained in Section 5. Section 6 presents the simulation findings and debates, while Section 7 presents the conclusion.

2. CONVENTIONAL LDO REGULATOR

The traditional (conventional) LDO regulator is explained in this section. Figure 1 depicts the traditional LDO regulator, which includes an error amplifier, a feedback network consisting of resistors R_1 and R_2, a PMOS pass transistor M_P, and a reference voltage, which is obtained from the band-gap reference circuits. The traditional LDO regulator compares the output voltage to the reference voltage and amplifies any differences using an error amplifier. The amplified differential voltage will modify the pass transistor overdrive voltage in order to keep the output voltage at the required level. The output voltage can be expressed in terms of reference voltage V_{ref} and feedback resistors R_1 and R_2. The output voltage of the traditional voltage LDO regulator in Figure 1 is given by,

$$V_{OUT} = V_{REF}\left[1 + \frac{R_1}{R2}\right] \tag{1}$$

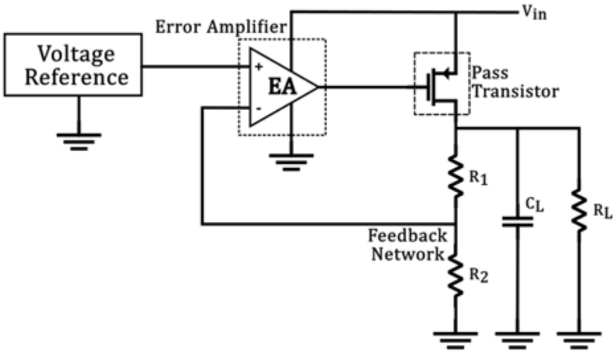

Figure 1. Traditional LDO regulator

The output voltage given in equation (1) will be independent of supply voltage and load currents if DC gain of EA is high. Figure 2 depicts the signal flow depiction of the traditional LDO regulator. The DC gain (Hinojo et al., 2018) with respect to V_{OUT} and V_{REF} is provided by,

$$\frac{V_{OUT}}{V_{REF}} = \frac{A_{EA}g_mR_L}{1+A_{EA}g_m\beta R_L+\frac{R_L}{r_o}} \tag{2}$$

If the DC gain of the EA and output stage is high, then the following assumption is true; this is given by,

$$A_{EA}g_mR_L >> 1$$

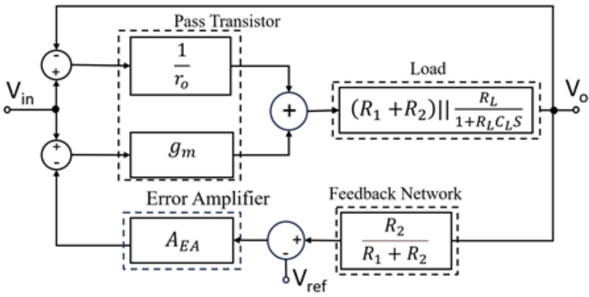

Figure 2. SFG of conventional LDO regulator

Where A_{EA} is the DC gain of the EA and g_mR_L is the DC gain of the output stage. If above constraint is true, then equation (2) can be simplified to

$$\frac{V_{OUT}}{V_{REF}} \approx \frac{1}{\beta} \tag{3}$$

The equation (3) is the same as equation (1). This indicates that the output voltage does not vary with the supply voltage and load currents.

Similarly, the DC transfer function with respect to V_{OUT} and V_{IN} is given by,

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_m R_L + \frac{R_L}{r_o}}{1 + A_{EA} g_m R_L \beta + \frac{R_L}{r_o}} \tag{4}$$

The equation (4) is further simplified into

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + g_m r_o}{1 + A_{EA} g_m r_o \beta + \frac{r_o}{R_L}} \tag{5}$$

Assuming the DC gain of the output stage is high, which is given by

$$g_m r_o >> 1$$

If the above constraint is true, then the equation (5) can be simplified to,

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{A_{EA}\beta} \tag{6}$$

The transconductance and output resistance of the pass transistor are represented by g_m and r_o respectively, along with the DC gain of the error amplifier A_{EA} and the feedback network β, which is given by the following expression

$$\beta = \frac{R_2}{R_1 + R_2} \tag{7}$$

Uncompensated LDO regulators have two substantial poles and one RHP zero, making them potentially unstable. The dominant pole is determined mostly by the error amplifier's output resistance and the pass transistor's parasitic capacitance. Additionally, the second pole (first non-dominant pole) is situated at the output node of the LDO regulator, and its location is dependent on the load condition. The first-order approximation ignores other poles produced by the error amplifier, as it assumes that these poles are located at very high frequencies. In addition, due to the large parasitic capacitor C_{gd} of the pass transistor, a feed-forward path is formed, which generates an RHP (Right-Half Plane) zero. Equations (8) and (9), respectively, give the dominant pole and the second pole based on [8], [9], [10].

$$\omega_{p1} = \frac{1}{R_I C_I} \tag{8}$$

Where R_I and C_I are the error amplifier's (first stage) output resistance and capacitance.

$$\omega_{p2} = \frac{1}{R_{II} C_{II}} \tag{9}$$

Where R_{II} and C_{II} are the error amplifier's (second stage) output resistance and capacitance. Where R_{II} is

$$R_{II} = r_o, p \,||R_L||(R_1 + R_2)$$

Where r_o,p is the small-signal resistance of the pass transistor Equation (10) describes the RHP zero generated by the feed-forward circuit.

$$\omega_{z1} = \frac{g_{m,p}}{C_{gd,p}} \tag{10}$$

The RHP zero of the LDO regulator is dependent on the load current. When the load current is large, the pass transistor's transconductance increases, causing zero to appear at a high frequency. Conversely, as the load current is reduced, the zero moves towards lower frequencies, which can make the LDO regulator prone to instability. Therefore, to ensure stability across all operating conditions, it is necessary to introduce frequency compensation network to stabilize the LDO regulator.

3. PROPOSED LDO REGULATOR

The proposed LDO regulator is explained in this section. Figure 3 depicts the block diagram for the proposed low dropout regulator. A multi-loop regulator regulates the input voltage V_{IN} from the power source or battery, resulting in a stable voltage V_{OUT}. The feedback network, error amplifier, and pass transistor make up the primary regulatory loop. The feedback network's job is to detect variations in V_{OUT}, which can occur as a result of changes in load current or unregulated supply voltage. The error amplifier compares the reference voltage V_{ref} to the feedback value, V_{fb} and regulates the pass transistor to keep the output voltage at the required level.

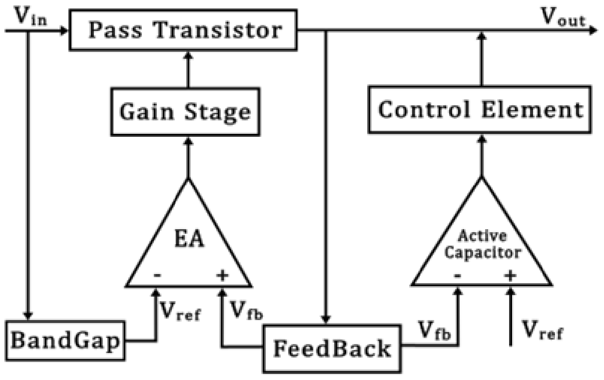

Figure 3. Block diagram of the proposed LDO regulator

Furthermore, this work suggests an active capacitor arrangement for transient augmentation at the output. This construction makes use of a fast comparator with offset voltage detection and increased closed-loop bandwidth to quickly alter the control element to either sink or source current to or from the output during fluctuations in unregulated supply voltage or load demands. This enhancement occurs without affecting the circuit's operation under static conditions and further accelerates transient performance without compromising circuit stability.

3.1 Error Amplifier

This sub-section explains the high-gain error amplifier. The DC gain of the error amplifier should be large in order to maintain better DC accuracy or to regulate the stable output voltage. In low dropout regulators, an error amplifier is critical part for maintaining output voltage stability and DC accuracy. It functions by comparing the output voltage of the low dropout regulator to a reference voltage, which is obtained from the band-gap reference and amplifying any difference or 'error' between them. The gate voltage of the pass transistor is subsequently modified using this amplified error signal, so regulating the output voltage in response to variations in the load current or input voltage. This feedback mechanism improves the overall performance and dependability of the voltage regulator by ensuring that the low dropout regulator compensates for any disruptions and maintains a consistent output voltage regardless of differences in load current or input supply. In this paper, the use of a CMOS symmetrical amplifier (Wan et al., 2019) as an error amplifier is crucial for the error detection and correction mechanism within the low dropout regulator. The symmetrical configuration of the CMOS amplifier allows for balanced operation, reducing distortion and improving linearity, which are essential for stable and precise voltage regulation. This setup enhances error signal detection by providing high gain and fast response times, which effectively corrects any deviation from the desired output voltage (Răducan et al., 2020).

The main disadvantage of the cascode symmetrical CMOS OTA is its limited output swing (Li et al., 2020). For this purpose, a folded-cascode amplifier is preferred. The circuit schematic of the folded-cascode amplifier is given in Figure 4. The transistors $M_{E1},\ and\ M_{E4} - M_{E5}$ are bias transistors, and the transistors $M_{E2} - M_{E3}$ form an input differential pair. The transistors M_{E6} and M_{E7} form the current buffers. The transistors M_{E8} to M_{E11} form a cascode current mirror. The cascode transistors are biased by a separate biasing network, which provides V_{BIAS-1},V_{BIAS-2},V_{BIAS-3}, and V_{BIAS-4}. Normally, the current through transistor M_{E4} is twice the current through transistor M_{E2}. As a result, the current through transistors $M_{E6} - M_{E11}$ is the same as through the input transistor $M_{E2} - M_{E3}$.

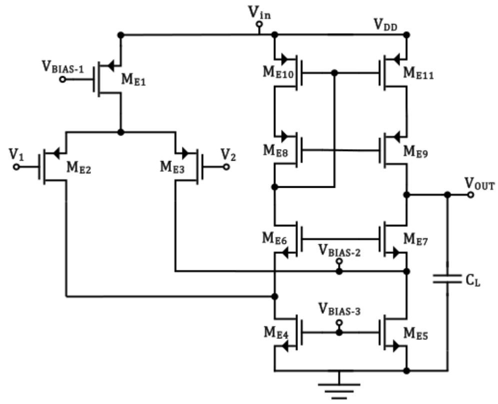

Figure 4. Folded Cascode Amplifier

If V_{IN} is the differential AC input voltage, the $\frac{g_{m2}V_{fb}}{2}$ is the AC current flowing in the input transistors. This current flows from transistor M_{E3} through transistor M_{E8} and is mirrored by transistors M_{E10} and M_{E11} through transistor M_{E9} to the output. The input differential pair (M_{E2} and M_{E3}) contributes overall transconductance of the error amplifier and cascade transistors M_{E5}, M_{E7} , M_{E9} and M_{E11} boosts the output resistance of the error amplifier. The output resistance R_{out} consists of a resistance towards M_{E9}, called, $R_{out\,7} = \frac{1}{g_{out7}}$ and one towards M_{E7}, called $R_{out\,7} = \frac{1}{g_{out6}}$. It is given by,

$$R_{out} = \frac{1}{g_{out6}} + \frac{1}{g_{out7}}, \text{ with}$$

$$g_{out7} = \frac{g_{09} \cdot g_{10}}{g_{m9}}, \text{ and}$$

$$g_{out6} = \frac{g_{07}\ (g_{o5} +\ g_{o2})}{g_{m7} +\ g_{mb7}}$$

The DC gain A_{VO} of the error amplifier is given by,

$$A_{VO}\ =\ g_{m2}.R_{out}$$

3.2 Active Capacitor Circuit

This sub-section examines the analysis of the suggested active capacitor circuit. In addition, the proposed paper introduces an auxiliary active capacitor circuit depicted in Figure 5. This circuit emulates the behavior of a high-capacity passive capacitor situated at the output of the LDO regulator, swiftly responding to variations in output voltage by providing immediate current support to stabilize these fluctuations during changes in load. This contrasts with the configuration in (Manikandan et al., 2021b), where the active capacitor is part of the LDO regulator's main loop. The current design uses a set of 12 transistors labelled M_{C1} through M_{C12} to implement this function.

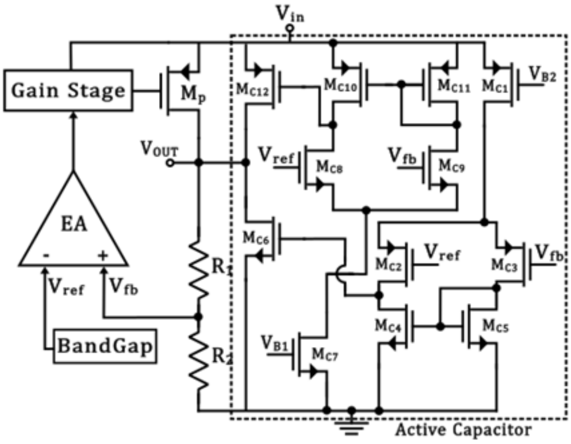

Figure 5. The proposed active capacitor circuit

Specifically, it features a rapid comparator circuit comprising transistors M_{C1} to M_{C5} that activates transistor M_{C6} to quickly dissipate excess charge during transitions from high to low load. Conversely, the comparator circuit consisting of transistors M_{C7} - M_{C11} activates transistor M_{C12} to bolster charge during shifts from low to high load. This ensures that the response times are quicker than those of the main loop due to the smaller dimensions of M_{C6} and M_{C12} compared to the main pass transistor M_P, enhancing the system's overall closed-loop bandwidth. The fast comparators have greater bandwidth than the main EA, allowing for faster response than the main loop.

The active capacitor circuit is specifically designed to activate only during voltage overshoots or voltage undershoots, which could potentially destabilize the system. This function is controlled by adjusting the input offset voltage of the rapid comparator. Under dynamic condition, when $V_{fb} \geq \ V_{ref} + V_{os,in}$, M_{C6} is turned on to source current from the output voltage V_{out}. Similarly, when $V_{fb} \leq V_{ref} - V_{os,in}$, M_{C12} is turned on to sink current into output voltage V_{out}, where $V_{os,in}$ is the input offset voltage of the fast comparator. In this configuration, the structure serves as an active capacitor at output voltage V_{OUT}, dynamically sourcing or sinking current as needed to stabilize the output voltage.

3.3 Proposed transistor level LDO regulator

This section explains the proposed LDO regulator's transistor-level implementation. Figure 6 depicts the proposed completely integrated LDO regulator with a rapid transient response. It also includes the error amplifier, pass transistor M_P, feedback network comprised of resistors R_1 and R_2, and an output load capacitor C_L, which can be an on-chip capacitor and the active capacitor circuit. The proposed LDO includes three gain stages. Stage 1 of the proposed LDO regulator is an error amplifier stage, which is implemented by the transistors $M_{E1} - M_{E11}$. Stage 2 is a basic common-source amplifier that is implemented by the transistors $M_{S1} - M_{S2}$. The final stage is an output stage, which is a typical amplifier stage that is implemented by the power transistor M_P. Each stage of a three-stage LDO regulator adds at least one LHP pole, causing a stability issue. The suggested LDO regulator requires a frequency compensation to stabilize the multi-stage LDO regulator. The suggested LDO regulator employs two compensation capacitors to stabilize the multi-stage LDO regulator during load changes. The LDO regulator is designed in such a way that the reference voltage is equal to feedback voltage. This is achieved through a non-unity feedback structure that uses feedback resistors and output voltage to determine the feedback voltage V_{fb}. The error amplifier senses the difference between the feedback voltage (V_{fb}) and the reference voltage (V_{ref}) and sends it to the gain stage. The signal is then applied to the gate of the pass transistor, which regulates the output voltage using negative feedback. The extra gain will raise the slew rate at the pass transistor's gate, improving the transient response of the LDO regulator. During load transients, the active capacitor circuit also acts as a rapid source or sink of current from or to the output capacitor. The active capacitor circuit has an offset voltage; therefore it has no effect on system stability. The previous section revealed that uncompensated LDO regulators are unstable. The miller capacitor is used in this design to address this issue (Gao et al., 2023), which is connected between the second stage and the output of the LDO regulator, and another feed-forward compensation capacitor is connected between the first stage and second stage of the LDO regulator. The miller capacitor C_{M2} creates the dominant pole for the LDO regulator, which is located at the second stage's output. The capacitor C_{F1} forms a feed-forward route and generates LHP zero, reducing negative phase and boosting stability by increasing phase and gain margins.

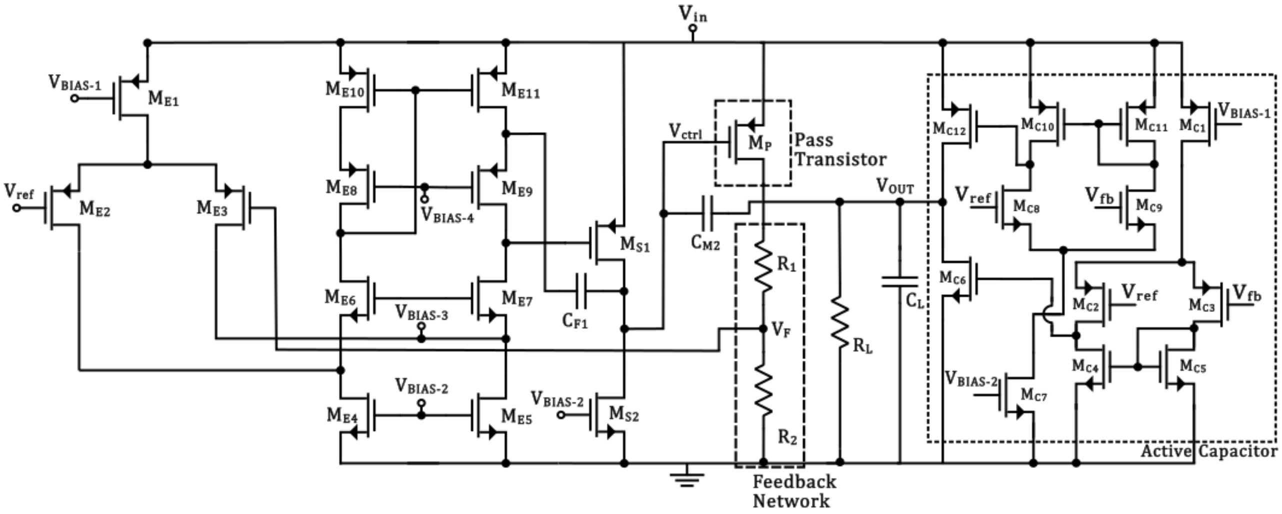

Figure 6. Proposed transistor level LDO with fast transient response

As compared to the NMOS pass transistor topology (Han & Lee, 2021; Răducan et al., 2020), which requires additional circuits and has more dropout voltage as compare to PMOS pass transistor. This design utilizes the PMOS pass transistor topology due to its lower dropout voltage and absence of any additional circuitry requirement. Usually, the dropout voltage for the PMOS topology ranges from 0.2V to 0.4V. The pass transistor should be correctly scaled to maintain the desired output voltage of 1.6 V despite supply and load changes. In the proposed work, the pass transistor is designed to regulate peak load currents of up to 50 mA with a dropout voltage of 0.2V from the unregulated supply voltage of 1.8 V. The high DC gain of the proposed LDO regulator ensures the output voltage is constant and independent of the variation in supply voltage and load current.

4. STABILITY ANALYSIS OF THE PROPOSED LDO REGULATOR

The stability study of the suggested LDO regulator is explained in this section. The LDO regulators must work in a wide range of load situations while ensuring the stability of the feedback loop. An unstabilized LDO regulator contains two major poles, as was previously mentioned in the section on traditional LDO regulators (Lee et al., 2022). The primary poles of the unstabilized LDO regulator are two. The massive parasitic capacitance at the gate of power transistor one of them. The second pole is positioned at the output node and is determined by the load circumstances. The error amplifier's remaining internal poles can be assumed to be relatively high-frequency poles, and their effect on the system can thus be ignored in a first-order approach. The suggested LDO regulator uses a folded-cascode as an error amplifier, resulting in a three-stage structure for the total capacitor-less low dropout regulator. The introduction of three gain stages improves the low frequency accuracy of the low dropout regulator and raises the DC value of the PSR (Zamora et al., 2020). Nonetheless, rigorous frequency adjustment must be implemented. Two compensation capacitors, $\boldsymbol{C_{F1}}$ and $\boldsymbol{C_{M2}}$, as indicated in Figure 6, are required. The dominating pole is placed at the output of the second stage via a miller compensation capacitor. The first non-dominant pole arises at the LDO regulator's output node, whereas the second non-dominant pole arrives at the EA's output, which occurs at high frequency and has no effect on small-signal performance. In conjunction with a miller capacitor, the feed-forward capacitor produces an LHP zero and stabilizes the LDO regulator.

5. TRANSIENT RESPONSE OF THE PROPOSED LDO REGULATOR

This section examines the proposed LDO regulator's transient response. An LDO regulator's output voltage can fluctuate due to rapid changes in both the input voltage and the load current. These cases are classified as line transient and load transient reactions, respectively. Analyzing these responses is complex, especially considering that the pass transistor, M_P may function in various operational regions depending on the load. For line transients, enhancing the Power Supply Rejection Ratio (PSR) typically leads to quicker and more effective mitigation of substantial input voltage changes. Regarding load transients, the output voltage's reaction time might be constrained by the dynamics of the Error Amplifier (EA) or the characteristics of the pass element. Specifically, when switching from a low to a high load current, the pass transistor's robust driving capacity quickly provides a significantly higher current to the load. In such instances, it's crucial to fine-tune the slew rate of the EA to ensure the pass transistor is driven effectively. Additionally, the integration of an active capacitor circuit is specifically designed to activate only during voltage overshoots or undershoots (Liu & Chen, 2020). This function is controlled by adjusting the input offset voltage of the rapid comparator. If the feedback voltage (V_{fb}) exceeds the reference voltage (V_{ref}), then transistor M_{C6} is engaged to supply current to the output (V_{OUT}). On the other hand, if V_{fb} falls below Vref minus Vos, transistor M_{C12} is activated to draw current from V_{OUT} (Limpisawas et al., 2022). This setup, which results in a very low quiescent current and a substantially greater current during the stated current load transition, has been implemented.

6. SIMULATION RESULTS AND DISCUSSIONS

The simulation results are given in this section. The suggested LDO is implemented with 180 nm CMOS technology and simulated in Cadence Virtuoso. Its design enables it to operate a peak load current of 50 mA while maintaining a stable regulated output voltage of 1.6 V. It also has a dropout voltage of 0.2 V from a 1.8 V power supply. The proposed LDO's stability is evaluated using frequency response graphs. The frequency response characteristic response of the LDO for the peak load current 50 mA is shown in Figure 7.

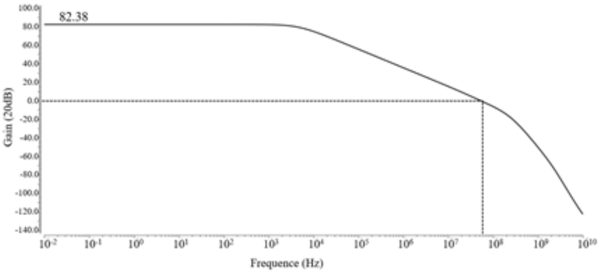

Figure 7. Gain vs Frequency plot of proposed LDO regulator

The suggested LDO regulator increases the LDO regulator's DC accuracy by achieving a maximum DC gain of 82.38 dB. The phase margin of the LDO regulator is determined by analyzing the bode plots shown in Figure 7 and 8, which is obtained with a load capacitance of 100 pF. At peak load of 50 mA, the phase margin of

62.2° is obtained. As the LDO regulator exhibits a positive phase margin under peak load conditions, it indicates that the proposed LDO regulator is operating in a stable condition.

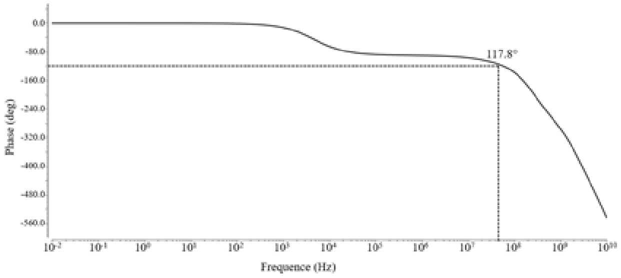

Figure 8. Phase vs frequency plot of proposed LDO

Line transient regulation analyzes the LDO's performance under supply volatility. The LDO regulator's line regulation under simulated conditions at a maximum load current of 50 mA is shown in Figure 9. The input voltage ranges between 2 V and 1.7 V for a reference voltage of 1.6 V, with rise and fall times of 100 ns. The voltage spike is measured to be approximately 190 mV. The proposed LDO regulator has a quiescent current consumption of 93 μA at a no-load condition. While it is desirable to reduce the quiescent current for better efficiency, doing so will unavoidably slow down the transient responses of the LDO regulator. The load regulation (LDR) is another important static specification of the LDO regulator.

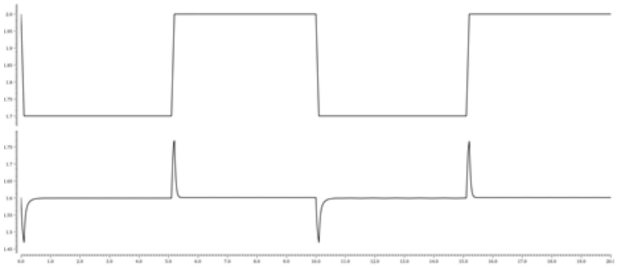

Figure 9. Line transient response of proposed LDO regulator

The load regulation of the proposed LDR, which is calculated using the given equation (11),

$$LDR = \frac{V_{Out@I-max} - V_{Out@I-min}}{I_{max} - I_{min}} \tag{11}$$

Using the equation (11) the 0.02 $\frac{\mu V}{mA}$ desired value of LDR is achieved. This small LDR ensures that the proposed LDO regulator performs better under load variations. The performance of the proposed LDO regulator is assessed using figure merits (FOMs). The FOMs described in (Manikandan et al., 2021b) are used for the comparison of the different LDO regulators, which is given by

$$FOM = T_s \frac{I_Q}{I_{L,max}} \tag{12}$$

Where T_s is the settling time, I_Q is the quiescent current $I_{L,max}$ is the maximum load current. The smaller is the FOM better is the transient response. The performance overview of the suggested LDO is displayed in Table 1 together with other recently released LDO regulators. Comparable performance is achieved by the proposed LDO regulator and the other reported LDO regulators.

Table 1. Performance summary of the proposed LDO regulator.

Specs	(Zamora, 2020)	(Manikandan, 2021a)	(Manikandan, 2021b)	(Gao et al., 2023)	**This work**
Technology (µm)	0.18	0.18	0.13	0.18	**0.18**
Year	2020	2021	2021	2023	**2024**
V_{IN} (V)	1.8	1.4	1.2	2-5	**1.8**
V_{OUT} (V)	1.6	1.2	1	1.8	**1.6**
$I_{L,max}$ (mA)	50	50	50	300	**50**
C_L (pF)	100	0-100	0-2000	5	**0-100**
ΔV_O (mV)	133	290	390	153	**190**
I_Q (µA)	95	55	95	66.4	**93**
FVF (ns)	4.58	0.66	0.38	0.09	**0.76**

7. CONCLUSION

The proposed LDO voltage regulator is a capacitor-less design with three stages and an active capacitor circuit for a fast transient response. It has been thoroughly analyzed and simulated in Cadence Virtuoso. The system is stabilized with two compensation capacitors, which enhances the phase margin, gain margin and makes the LDO regulator stable for the entire load ranges. The designed LDO regulator consistently regulated the output voltage of 1.6 V for the load current ranges of 100 μA–50 mA. The proposed LDO regulator regulates the output voltage of 1.6 V from the unregulated power supply voltage of 1.8 V with a dropout voltage of 0.2 V, and the total quiescent current consumption is 93 μA. Simulation results indicate that the proposed LDO architecture is a suitable building block for any system-on-chip application that requires medium-current loads.

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