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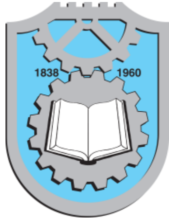

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SCHMITT TRIGGER BASED NVSRAM CELL FOR LOW POWER MOBILE SYSTEMS

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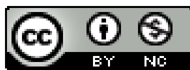

A B S T R A C T

The power saving in mobile systems is a big concern. It has attracted the attention of most of the researchers. In addition to this, process variation plays an important role in device performance, especially at lower technology nodes and low supply voltages. The application of non-volatile memory (NVM) devices with SRAM cell is found as an effective solution for power consumption. Also, the Schmitt Trigger (ST) action helps in maintaining the device performance under process variations. To attain both the features, a non-volatile SRAM (nvSRAM) cell using eleven transistor and one memristor (11T1M) is presented in this work. In addition to this, Schmitt Trigger (ST) action is used to improve the stability of the proposed design. From simulations, it is observed that the proposed 11T1M nvSRAM cell offer minimum deviation in delay performance and better stability in comparison to considered cells. The leakage power consumption of proposed design is also minimum.

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1. INTRODUCTION

The advancement in technology has increased the inconsistency between processor and memory and many methods are introduced to reduces this memory and storage bottleneck (Barbosa & Alves, 2011; Petersen et al., 2008) . One of the possible ways is modifying the memory architecture such as a radical memory-centric architecture (Faraboschi et al., 2015). In this, the data is accessed directly instead of indirect block oriented-path which is used in today's systems. The non-volatile memory (NVM) devices are suitable for such architectures (Puglia et al., 2019). The Flash memory is commonly used NVM device in computing systems. However, it is not the best fit due to increased complexity and cost (Kurata & Gastaldi, 2010). There are other NVM devices also such as MRAM, FeRAM, PCM, memristor, which meets the expending needs of application requirements and are cost effective (Meena et al., 2014). Among these devices, memristor is found suitable due to its fast-operating speed, small size and compatibility with CMOS technology.

The performance of mobile devices is directly dependent on the technology and voltage scaling as most of the chip area is occupied by SRAM cells (Jawar Singh et al., 2013). It leads to reduced power consumption at the cost of increased leakage and read/write access time. To reduce leakage, turning OFF the device is not possible when SRAM is in idle state due to its volatile nature. Owing to this, memristor is integrated with SRAM cells to make it non-volatile (Huang & Lian, 2013). It is vertically connected to internal node of the cell so that there is parallel and fast transmission of data (Chang et al., 2012). The non-volatile SRAM or nvSRAM cell not only

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provides data storage in non-volatile manner but also gives low power operations.

In literature, there are several nvSRAM cells which differ in connection of memristor. In 6T2R cell (Wang et al., 2006), memristor is directly connected to internal nodes of conventional 6T SRAM cell which causes leakage in the cell and reduced stability. The 7T2R cell (Sheu et al., 2013) controls the memristor operation through a transistor which increases the cell stability, however, the leakage issue is still there. To reduce leakage, the 8T2R cell is introduced (Turkyilmaz et al., 2012, 2014) in which one transistor and one memristor (1T1M) cell is connected to both internal nodes. This cell further enhances the stability of the cell; however, it's application is limited due to high energy consumption. In Rnv8T2R cell (Chiu et al., 2012), the control transistors are connected to bitline pair which gives the parallel write path and reduces the write delay. It also enhances the stability; however, the direct connection with bitline pair increases the leakage in the cell. Also, the store/restore operation is very complex. To overcome these issues, 7T1R cell (Wei et al., 2014) is introduced in which 1T1M cell is connected to internal node Q only. It gives the advantage of instant ON and reduces energy consumption. To enhance the restore performance and further reduce energy consumption, IOW 7T1R cell (Lee et al., 2015) is introduced. It uses differential supply voltage and initialized and overwrite (IOW) scheme. It improves the read/write stability of the cell also. The Avg. 7T1R cell (Peng et al., 2018) uses column shared technique to further enhance the read/write margin and reduces the energy consumption. To further enhance the restore and read/write performance, RD 8T1R cell is introduced in (Lin et al., 2019). It uses shared per technique to improve restore and write performances and isolated read port to improve read performance. The MS 7T1R cell (Lin et al., 2020) and MS 8T1M cell (D. Singh, Pandey, et al., 2022) perform single ended write operation and save the write power upto an extent. In MS 7T1R cell (Lin et al., 2020), the pass transistor is used to perform write operation, while in MS 8T1M cell (D. Singh, Pandey, et al., 2022), the pass transistor is replaced by a transmission gate (TG). The read and store/restore performances of both the cells are similar to RD 8T1R cell (Lin et al., 2019). These cells reduce the read delay also; however, it is dependent on memristor state completely. In 8T1M cell (D. Singh, Gupta, et al., 2022a), the read operation is differential and write operation is single ended. It is done with the help of a feedback transistor which turns ON during read operation and remain OFF during write operation. Although, this cell reduces the write power consumption, the delay performance is degraded. In RD 8T1M cell (D. Singh, Gupta, et al., 2022b), one of the pull-down transistors is turned OFF to improve the write performance, but it also causes leakage in the cell. Also, the read assist circuit is used to enhance the read performance of the cell. In 7T2M cell (Jeetendra Singh & Raj, 2019) and 8T3R cell (Janniekode et al., 2022), the memristor is connected to pull-down transistor which enhances the stability of the cell. In 7T2M cell (Jeetendra Singh & Raj, 2019), 1T1M structure is connected to internal node Q only, while in 8T3R cell (Janniekode et al., 2022), 1T1M structure is attached to both the internal nodes of the cell. The 8T1R cell in (Bazzi et al., 2021) is introduced for low power application, however, the direct connection of memristor to internal node for the cell reduces the stability of the cell.

The detailed investigation on existing nvSRAM cells indicate that the customary work is done on improvement of stability, write/store/restore performances and reduction of leakage. The delay performance is also an important issue and less attention is paid in this area. It is required that the speed of the nvSRAM cell remain maintained with technology scaling, else, there may exist a time slack during transmission of data between cell and processor. Further, the process variation is also an important issue in small geometry devices. With scaling in the device dimensions, the inter-die and intra-die variations become dominant which may change the threshold voltage of the transistor (Bhavnagarwala et al., 2001; Kulkarni et al., 2007, 2012; Nakagome et al., 2003). It leads to degradation in cell performance. So, it is necessary to make cell tolerant against process variations. In this work, a Schmitt Trigger (ST) based 11 transistor and 1 memristor (11T1M) nvSRAM cell is introduced. The primary objective of this work is to make the cell process invariant and improve the delay performance, while maintaining the stability of the cell. The following are the salient features of this work:

1. The ST inverter is used to make the proposed nvSRAM cell tolerant against process variations.
2. The negative Vss technique is used to reduce the read delay of the cell. It also supports in improvement of cell read stability.
3. The complexity during store/restore operation is avoided in the proposed cell.

The rest of the work is organized as follows: Section 2 explains the working of proposed ST 11T1M nvSRAM cell is detail. In section 3, the performance analysis of the proposed design is carried out and the results are compared with considered nvSRAM cells. The last section 4 concludes the work.

2. PROPOSED ST 11T1M NVSRAM CELL

The diagrammatic representation of proposed ST 11T1M nvSRAM cell is shown in Figure 1. It incorporates two ST inverters (Inverter1: PDL1-PDL2-FBL-PUL and In-verter2: PDR1-PDR2-FBR-PUR) which are coupled together to store data at internal nodes Q and QB. The write access transistors ACL and ACR are controlled by write wordline WWL, while the feedback transistors FBL and FBR are controlled by word-line WL. The WWL line is activated during write operation only while, the WL line is activated during both write and read operations. The WBL and WBLB

are complementary bitlines. The pass transistor PG is controlled by control signal CTL1 and controls non-volatile operation through memristor M1 via control signal CTL2.

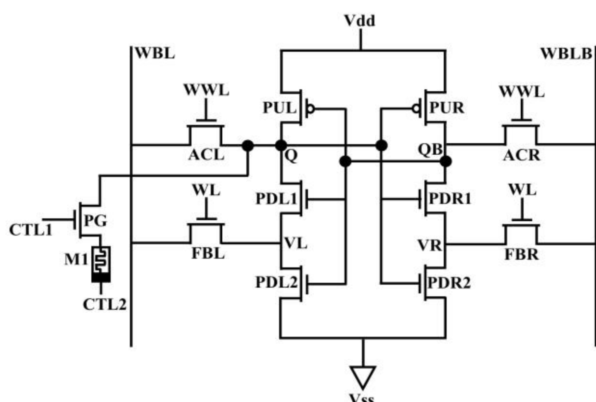


Figure 1. Proposed ST 11T1M nvSRAM cell

The proposed design performs differential write and read operations. The ST action is performed through feedback transistor FBL/FBR by asserting WL line. It im-proves the proposed design's stability during both write and read operations. The status of different signals during different operation is given in Table 1.

Table 1. Status of control signals during different operations

Operations	Control Signals			
	WWL	WL	CTL1	CTL2
Write	"HIGH"	"HIGH"	"LOW"	"LOW"
Read	"LOW"	"HIGH"	"LOW"	"LOW"
Hold	"LOW"	"LOW"	"LOW"	"LOW"
Store	"LOW"	"LOW"	"HIGH"	"LOW"
Power - Down	"LOW"	"LOW"	"LOW"	"LOW"
Restore	"LOW"	"LOW"	"HIGH"	"HIGH"

2.1 Write operation

To write content at internal nodes, the signals are asserted as tabulated in Table 1. For writing '1', the precharged WBLB line is discharged, while WBL line remain at "Vdd". The internal node Q is charged to "Vdd" via transistor ACL and bitline WBL. The FBL transistor increases threshold voltage of pull-down transistor PDL1 and reduces its driving capability that supports charging of internal node Q. On the contrary, the internal node QB is discharged quickly due to existence of two current dis-charge path (one path through ACR and another path through FBR). Due to the balanced configuration of the proposed design, write '0' operation is performed in similar manner.

2.2 Read operation

To perform read operation, the control signals are asserted as tabulated in Table 1 and the Vss line is pulled to negative voltage. When logic '1' is stored at internal node Q, the pull-down transistor PDR1 and PDR2 are turned ON. It discharges precharged WBLB line through transistor FBR to transistor PDR2. The negative Vss increases the read current and fasten the discharging of WBLB line. On the other side, the precharged bitline WBL remain at Vdd as PDL1 and PDL2 are OFF. The difference be-tween bitline pair WBL and WBLB is sensed to complete read '1' operation. The similar process is followed to perform read '0' operation. Further, the feedback transistors activate the ST action with assertion of WL signal which prevents the flipping of cell data during read operation. In addition to this, the isolation of bitline pair (WBL and WBLB) to internal nodes (Q and QB) increase the cell stability during read operation and hence the read margin is enhanced.

2.3 Hold operation

To hold data, the internal nodes are isolated from bitline pair by de-asserting signals WWL and WL. The ST action is absent during hold mode as feedback transistors are OFF and the hold stability completely depends on feedback connection of ST inverters. The series of two NMOS transistor weaken the pull-down path and increases hold stability of the cell.

2.4 Store operation

Prior to store operation, memristor is initialized to High Resistance State (HRS). The combination of transistor PG and memristor M1 is associated with node Q. Due to the logic '1' stored at node Q, memristor M1 changes its state from HRS to LRS (Low Resistance State). If logic '0' is present at node Q, memristor M1 retain HRS state.

2.5 Power – Down operation

During power down, the internal nodes Q and QB lose their content due to the absence of power supply. However, memristor M1 retain its previous state due to its non-volatile nature.

2.6 Restore operation

In restore operation, the power supply is turned on again and the previous content of internal node is retrieved from memristor. The logic '1' can be recovered at node Q by charging it through memristor that is in LRS state. However, the charging of node Q is not possible through HRS state of memristor and logic '0' is recovered.

3. RESULT AND DISCUSSION

The proposed ST 11T1M nvSRAM cell is simulated using 32nm PTM model with the linear memristor model mentioned in (Biolek et al., 2013). The timing waveform during different operations of

proposed design is shown in Figure 2. The analysis is carried out in terms of delay, margin, failure probability and power consumption. The dimension (W/L) of all transistors is kept same i.e., 72nm/36nm.

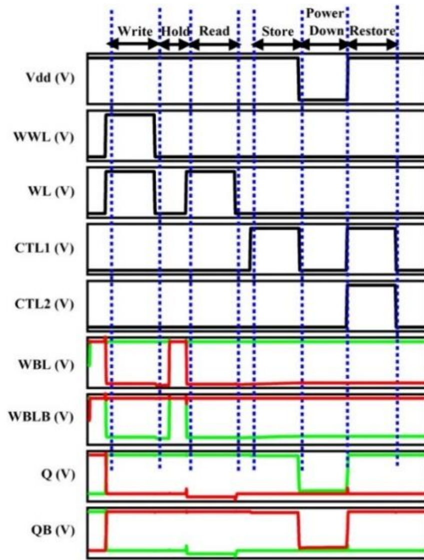


Figure 2. Timing waveform of proposed ST 11T1M nvSRAM cell for different operations (*Note: green line represents logic ‘1’ and red line represents logic ‘0’)

3.1. Write performance

In proposed design, the weak pull-down path supports charging of internal node, while on the other side, the feedback transistor gives an extra path for discharging. The overall effect reduces write delay of proposed design. The simulation results show that the write delay of proposed design is decreased by 19.21% at Vdd= 1.0V than the considered nvSRAM cells. It is also observed that the write margin of proposed design is enhanced by 30.15% and it shows minimum failure probability in comparison to considered nvSRAM cells. However, there is an increment of 20.63% in write power consumption of proposed design. The results for write performance of proposed and considered nvSRAM cells are shown in Figure 3.

3.2. Read performance

In proposed cell, the read path consists of feedback transistor FBL/FBR and pull-down transistor PDL2/PDR2. In existing Avg.7T1R (Peng et al., 2018), 7T2M (Jeetendra Singh & Raj, 2019), 8T1R (Bazzi et al., 2021) and 8T3R (Janniekode et al., 2022) nvSRAM cells, the read path is followed by access transistor to pull-down transistor. Hence, the proposed design shows reduction of 17.5% in read delay in comparison to considered nvSRAM cells at Vdd=1.0V. Also, there is an improvement of 33.33% in read margin of proposed design at same supply voltage and shows minimum failure probability in comparison to considered nvSRAM cells. However, there is an increment 10.5% in read power consumption of proposed design. The results for read performance of proposed design and considered nvSRAM cells are shown in Figure 4.

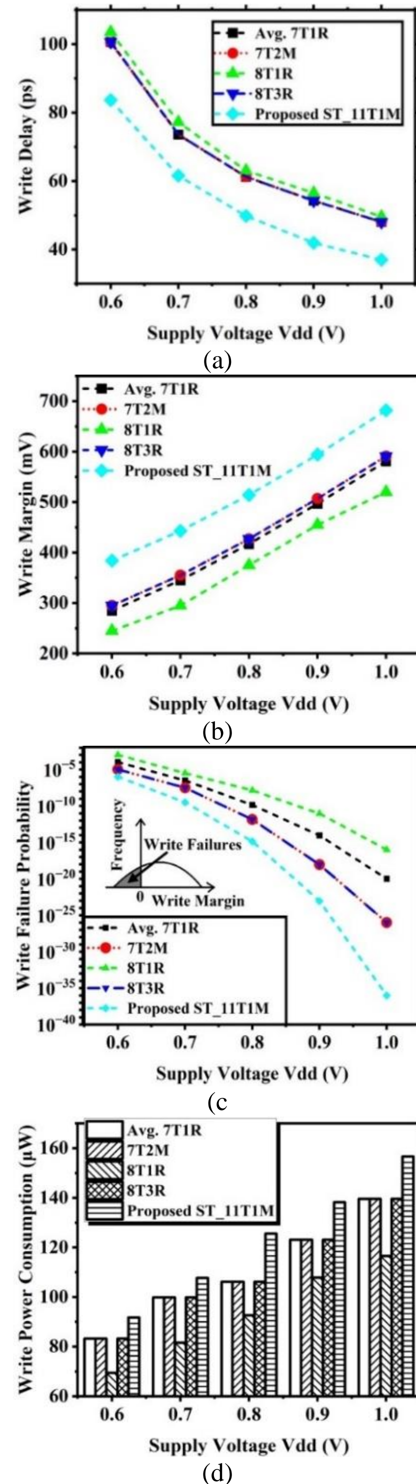


Figure 3. Write performance analysis for of proposed and considered nvSRAM cells; (a) write delay (b) write margin (c) write failure probability and (d) write power consumption

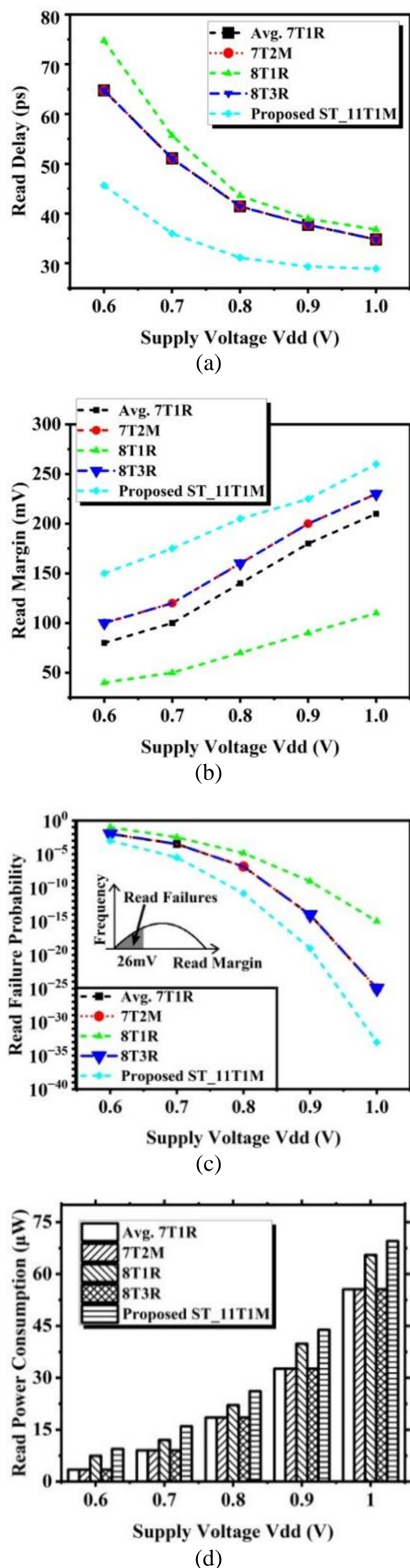


Figure 4. Read performance analysis for proposed and considered nvSRAM cells; (a) read delay (b) read margin (c) read failure probability and (d) read power consumption

3.3. Hold performance

The leakage power consumption analysis is carried out to evaluate hold performance and the result is presented in Figure 5. It is noted that the stacking of pull-down transistor reduces the driving capability and leads to reduction in leakage power consumption. The proposed design shows the reduction of 35.6% in leakage power consumption at Vdd=1.0V in comparison to considered nvSRAM cells.

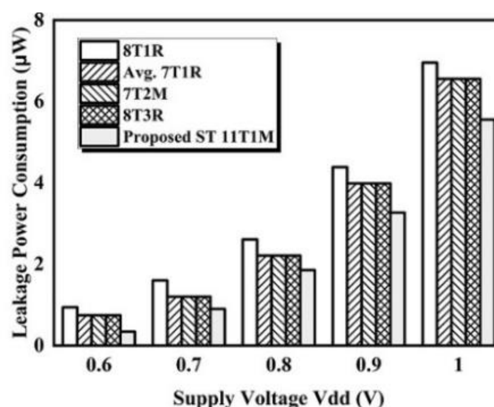


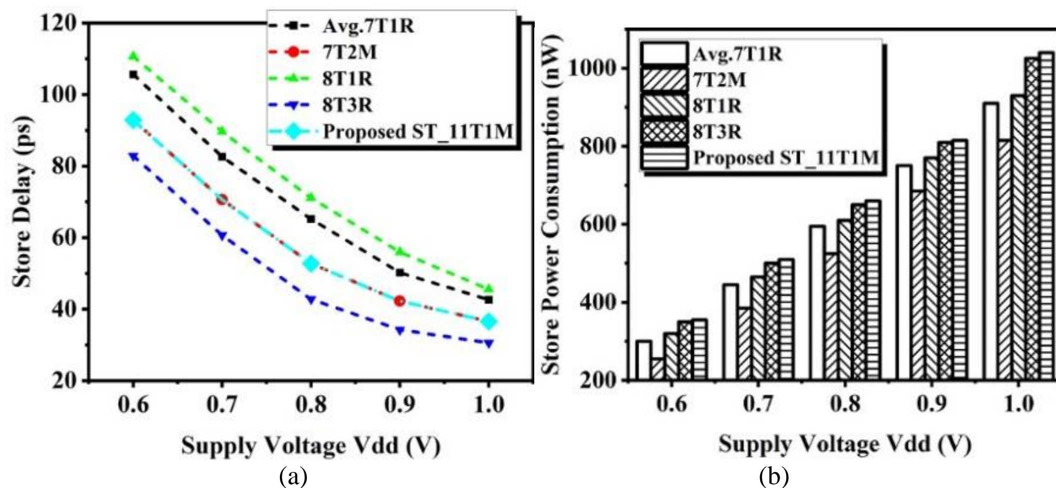
Figure 5. Leakage power consumption of proposed and existing nvSRAM cells

3.4. Store performance

The store performance is analysed in terms of store delay and store power consumption. The existing Avg.7T1R cell (Peng et al., 2018), 8T1R cell (Bazzi et al., 2021) need set and reset subphases to change the memristor state and it leads to increased store delay and store power consumption. In 7T2M (Jeetendra Singh & Raj, 2019), 8T3R (Janniekode et al., 2022) and proposed cell, such subphases are not required, leading to minimum store delay. The memristor state is dependent on control signal CTL1 and CTL2. The store delay and power consumption for proposed design and considered nvSRAM cells is shown in Figure 6.

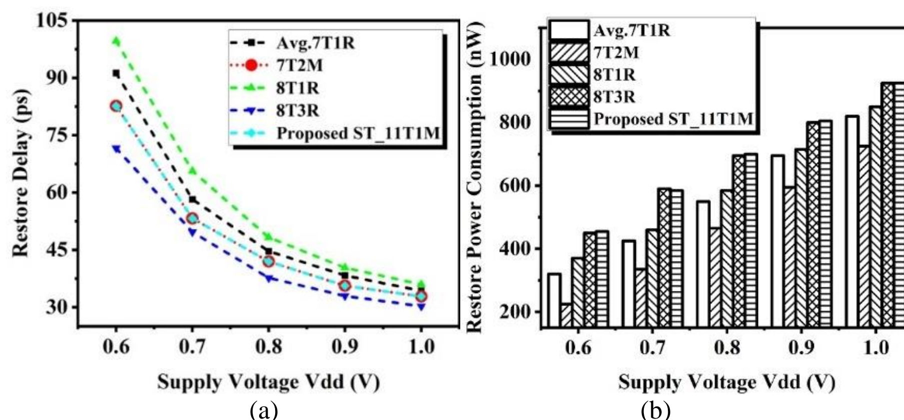
3.5. Restore performance

The restore performance is analysed in terms of restore delay and restore power consumption. In Avg.7T1R cell (Peng et al., 2018), 8T1R cell (Bazzi et al., 2021), the restore operation require subphases and change in power supply; leading to increase in restore delay and restore power consumption. While in 7T2M (Jeetendra Singh & Raj, 2019), 8T3R (Janniekode et al., 2022) and proposed design, the restore operation does not require subphases or change is power supply. The restore operation is performed using control signals CTL1 and CTL2. This causes reduction is restore delay and restore power of proposed design and the same can be observed from Figure 7.



(a) (b)

Figure 6. Store performance analysis for proposed and considered nvSRAM cells (a) store delay and (b) store power consumption



(a) (b)

Figure 7. Restore performance analysis for proposed and considered nvSRAM cells (a) restore delay and (b) restore power consumption

4. CONCLUSION

This paper presents non-volatile ST 11T1M nvSRAM cell that uses ST action to avoid the effect of process variation. The feedback transistor and stacking of pull-down network helps in maintaining the stability of the proposed design under process variations. In addition to this, the proposed design shows minimum leakage power consumption in comparison to considered nvSRAM cells. Also, from failure probability analysis, it is observed that the failure probability of proposed design is minimum during write and read operations. The combination of a transistor and a TiO_2 based memristor is used to perform store and restore operation.

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